Remarks

Reconsideration of pending Claims 1-149 is respectfully requested.

Information Disclosure Statement.

Enclosed herewith is a copy of the Information Disclosure Statement and Form 1449/PTO that were submitted by Applicant on December 3, 2002. Also enclosed is the PTO-stamped return postcard indicating receipt of the IDS in the USPTO.

The Examiner is respectfully requested to return the Form PTO-1449 in the next communication to Applicant, showing the citations as initialed and considered. Since the IDS' was filed prior to the issuance of a first office action on the merits, no fee is due for consideration of the listed items.

Restriction Requirement

The Examiner has indicated that the requirement for restriction is made final.[1] Reconsideration is respectfully requested for the following reasons:

1) The Examiner has raised a new issue that Claims 1, 2-6, 7-110, and 111-149 "are related as species subcombination which shown to be separately usable."

Applicant is unclear as to how these *method* claims relate to a "*species subcombination*" with relation to pending Claim 2 and with relation to each other.

The Examiner is respectfully directed to the discussion below at point 4) which lists and summarizes Claims 3-6 and 111-149.[2]

Applicant requests an explanation as to the basis for the Examiner's contention.

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[1] See Office Action at page 2 (emphasis added):

"Election/Restrictions

Applicant's election with traverse of claims 2-6 and 111-149 in Paper No. 11 is acknowledged. This is not found persuasive because the claims 1, 2-6, 7 110, and 111 149 are distinct species each other. **They are related as species subcombination which shown to be separately usable.** The distinct species have restricted in the last restriction requirement which including the species restriction of claims 111 149 (p.3).

The requirement is still deemed proper and therefore made FINAL."

[2] Claim 2 is to a method comprising three recited steps. Claims 3-6 (examined herein) and Claims 111-147 (*not* examined) depend either directly or indirectly from Claim 2.

2) *The Examiner has not shown by way of example that one of the subcombinations has utility other than in the disclosed combination.*

The Examiner is respectfully directed to MPEP 806.05(d) Subcombinations Usable Together (emphasis added):

806.05(d) Subcombinations Usable Together

Two or more claimed subcombinations, disclosed as usable together in a single combination, and which can be shown to be separately usable, are usually distinct from each other.

...

Form paragraph 8.16 may be used in restriction requirements between subcombinations.

§ 8.16 Subcombinations, Usable Together

Inventions [1] and [2] are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. **In the instant case invention [3] has separate utility such as [4].** See MPEP § 806.05(d).

...

The examiner must show, by way of example, that one of the subcombinations has utility other than in the disclosed combination. ...

The burden is on the examiner to provide an example.

If applicant proves or provides an argument, supported by facts, that the other use, suggested by the examiner, cannot be accomplished or is not reasonable, the burden is on the examiner to document a viable alternative use or withdraw the requirement.

The Examiner has failed to provide any support for his refusal to consider Claims 1, 2-6, 7-110, and 111-149 on the issue of "species subcombination which shown to be separately usable."

3) *The Examiner has failed to properly respond to the reasons and arguments advanced by Applicant in the traverse, as required under MPEP § 821.01.*

Section 821.01, in parts relevant to this discussion, recites as follows:

821.01 After Election With Traverse

Where the initial requirement is traversed, it should be reconsidered. If, upon reconsideration, the examiner is still of the opinion that restriction is proper, it should be repeated and made final in the next Office action. (See MPEP § 803.01.) **In doing so, the examiner should reply to the *reasons or arguments advanced by applicant in the traverse.*** Form paragraph 8.25 should be used to make a restriction requirement final.

In the Third Response to Restriction (filed March 25, 2003), Applicant distinctly and specifically set forth specific errors in the restriction requirement by the Examiner, which have not been properly considered nor addressed by the Examiner.

In addition, the Examiner has failed to clearly set forth a fully reasoned response as to why each of the depending Claims 111-149 is not readable on Claim 2 of the elected invention. See further discussion below at point 4).

4) *The Examiner erroneously maintains that no claim is generic.*

Under MPEP § 805.04(d) Definition of a Generic Claim,[3] Claim 2 should be properly deemed generic to Claims 3-6 and 111-149 for the following reasons:

- Claim 2 recites no material element additional to the elements recited in the depending Claims 3-6 and 111-147 or the independent Claims 148-149.[4]
- Claim 2 does not include material limitations in addition to those recited in each of Claims 3-6 and 111-147.
- Each of the *depending* claims 3-6 and 111-147 require all of the steps (*contain all of the limitations*) of the generic claim — Claim 2, and cannot be practiced without the steps of Claim 2.

(Note: Claims 2-6 are presently pending and have been examined herein. Claims 111-147 (not examined) depend either directly or indirectly from Claim 2.)

Claim 3: further defines the step of annealing the polysilicon substrate.
Claims 140, 145-146: further define the step of annealing.
Claim 4: further defines the polysilicon layer.
Claim 124: further defines the polysilicon layer.
Claims 5-6: further define the oxynitride layer.
Claim 147: further defines the oxynitride layer.

Claims 111-114: further define the step of nitridizing and the nitrogen-containing gas.
Claim 115: further defines the oxynitride and nitride layers.

[3] See Applicant's Third Response to Restriction at pages 2-4.

[4] See footnote 2.

Claim 116-118, 125-126, 138-139: further define the dielectric layer.
Claim 123, 141-144: further define the step of nitridizing.

Claims 119-122: add the additional step of annealing in an oxidizing gas.
Claim 127: adds the additional step of forming an opening in an insulative layer.
Claims 128-129: add the additional step of forming the polysilicon layer.
Claims 130-132: adds the additional step of providing a substrate.
Claims 133-137: add the additional step of forming an electrode layer/defining the layer.

- Likewise, *independent* Claims 148-149 contain all of the limitations of the generic claim — Claim 2.

Claim 148: essentially recites each of the limitations of Claim 2.
Claim 149: essentially recites each of the limitations of Claim 2, and adds the additional step of exposing the dielectric layer to an oxidizing gas.

Accordingly, Claim 2 should be considered as generic to claims 3-6 and 111-147, which should be considered by the Examiner in this application. Reconsideration and withdrawal of the Examiner's decision on the restriction is requested.

Rejection of Claims under 35 U.S.C. §103(a)

The Examiner rejected Claims 2-6 as obvious over Aronowitz (USP 6,033,998) in view of Kim (USP 5,464,783). This rejection is respectfully traversed.

The Examiner maintains the rejection of the claims on the basis that it would be obvious to modify Aronowitz's process in view of Kim's disclosure (a) to anneal the polysilicon substrate at a temperature of 800°C. (regarding Claims 2-3), and (b) to incorporate "a doped polysilicon substrate, to let oxide react with the underlying [sic] in order to reduce the overall dielectric constant and cell capacitance" (regarding Claim 4). The Examiner also contends that the selection of reaction parameters such as temperature and concentration would be obvious on the basis that "concentrate, temperature, thickness and concentration are considered to involve routine optimization," citing to *In re Aller*, 105 USPQ 233, 255 (CCPA 1955) (regarding Claims 2-3 and 5-6).

Aronowitz is directed to fabricating gate dielectric layers having variable thicknesses and composition over different regions of a semiconductor wafer. In particular, Aronowitz is

directed to solving the problem of "hardening" the gate oxide. Aronowitz addresses conventional methods for hardening gate oxides, and the shortcomings of those methods (at col. 2, lines 11 to col. 3, line 65).

To overcome the existing problems and to produce gate oxide (dielectric) layers having variable thicknesses, Aronowitz teaches (at col. 4, lines 12-28:

a) growing a gate oxide layer over a semiconductor wafer;

b) masking a region of the gate oxide layer;

c) nitridizing the unmasked gate oxide region to form an oxynitride layer over the gate oxide region;

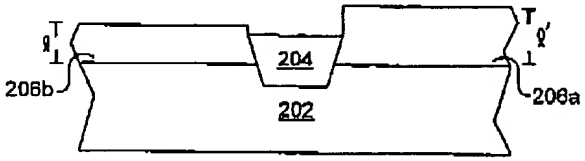
d) removing the mask; and

e) exposing the wafer to oxidation.

Aronowitz does not teach or suggest Applicant's method of forming a dielectric layer by *nitridizing the oxynitride layer* to form a nitride layer, and depositing a dielectric layer *onto the nitride layer*.[5]

Rather, Aronowitz teaches *exposing the wafer to oxidation* so that a dielectric layer is formed over and increases the thickness of the previously masked gate oxide region (206a) to thickness l' — but not the oxynitride layer and gate oxide region 206b. This is illustrated in FIG. 2F, and described by Aronowitz at cols. 6, line 61 to col. 7, line 6, bridging paragraph (emphasis added):

FIG. 2F



Then, the wafer is exposed to further oxidation according to methods well known in the art, such as thermal treatment. As shown in FIG. 2F, the oxynitrides which have been formed in the region 206b of the gate dielectric act as a barrier to the oxidation process. No such barrier exists in the un-nitridized region 206a of the gate dielectric. Consequently, different oxide

[5] Claim 2 recites: A method of forming a dielectric layer, comprising the steps of:
annealing a polysilicon substrate in nitric oxide at a temperature of less than 800°C. to form an oxynitride layer;
nitridizing the oxynitride layer to form a nitride layer; and
depositing the dielectric layer onto the nitride layer.

thicknesses can be grown on the same wafer: Thinner and hardened where nitridization has been performed, and thicker and not hardened in those regions that were masked during the nitridization. As shown in FIG. 2F, the nitridized region 206a of the gate dielectric has a thickness designated 1. The un-nitridized region 206b has a thickness designated 1', which is greater than 1.

See also the description in the Summary at col. 4, lines 40-45 (emphasis added):

In one aspect, the present invention provides a method of making a variable thickness gate dielectric. The method includes providing an initial gate oxide layer on a semiconductor wafer substrate, forming a mask over a portion of the initial gate oxide where a thicker dielectric is to be formed, and nitridizing the unmasked portion of the initial gate oxide by a technique which localizes nitrogen proximate to a top surface of the initial gate oxide layer...The mask is then removed and the wafer is exposed to further oxidation. In this way, oxynitrides formed in the previously unmasked portion of the initial gate oxide layer act as a barrier to the oxidation process so that the further oxidation of the wafer produces a thicker dielectric layer in that portion of the initial gate oxide that was masked during the nitridization. Variable thickness gate dielectrics in accordance with the present invention may be particularly advantageous in semiconductor integrated circuits involving both digital and analog devices.

Thus Aronowitz essentially *teaches away* from the present method, i.e., *nitridizing the oxynitride layer* to form a nitride layer, and depositing a dielectric layer *onto the nitride layer*.

A reference teaches away when "a person of ordinary skill, upon reading the reference ... would be led in a direction divergent from the path that was taken by the applicant." *In re Gurley*, 313 USPQ2d 1130, 1131 (Fed. Cir. 1994).

Throughout the disclosure, Aronowitz emphasizes the oxidation of portions of the wafer (e.g., gate oxide region 206a) to form variable thickness gate dielectric in different regions of the wafer. See above and at col. 5, lines 29-31.[6]

As such, Aronowitz teaches away from Applicant's method as claimed.

Based on the teaching of Aronowitz, one of skill in the art would have no motivation or basis to *nitridize* an oxynitride layer, and deposit a dielectric layer onto the nitride layer overlying the oxynitride layer as claimed.

[6] Aronowitz at col. 5, lines 29-31: "In the previously unmasked regions, thin but highly concentrated oxynitrides have been formed. These act as a barrier to the oxidation process. Consequently, different oxide thicknesses can be grown on the same wafer, thinner and hardened where nitridization has been performed, and thicker and not hardened in those regions that were masked during the nitridization..."

Furthermore, there is no motivation to combine Aronowitz with the teachings of Kim as proposed by the Examiner.

Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Here, Aronowitz expressly and directly *teaches away* from any combination with Kim's process.

In fact, Aronowitz not only cites Kim (USP 5,464,783) but points out the failures and disadvantages of Kim's process. See BACKGROUND OF THE INVENTION at col. 3, lines 29-45 (emphasis added)

> .....
>
> Composite dielectric layers have also been proposed, for example, by U.S. Pat. Nos. 5,258,333 and 5,464,783. The '333 patent discloses a process of thermal nitridization of a silicon substrate in pure ammonia, followed by CVD deposition and optional thermal nitridization in N_2 of a high temperature oxide layer. ***The '783 patent involves the formation of an oxynitride layer on a silicon substrate, such as by a thermal anneal in an oxygen and nitrogen-containing atmosphere or by a CVD system using oxygen and nitrogen with silane, dichlorosilane, disilane, or $SiCl_4$ followed by a thermal oxidation step to form an oxide layer at the substrate-oxynitride interface. However, the processes described in these patents rely upon nitridization techniques which do not provide a high degree of control over the incorporation of nitrogen in an oxynitride layer, and are unable to achieve high levels of nitrogen incorporation (i.e., greater than about 10%) in the final oxynitride layer of the composite.***
>
> .....

Aronowitz explicitly describes Kim's process as being undesirable. In the face of this, one skilled in the art would not be expected to combine the teachings of Aronowitz with Kim.

Furthermore, the teachings of Aronowitz and Kim are inconsistent and contain no suggestion or incentive in support of the Examiner's proposed combination of the two references.

Kim is directed to a process for forming an oxynitride-dioxide composite gate dielectric. The dual layer gate dielectric is formed by

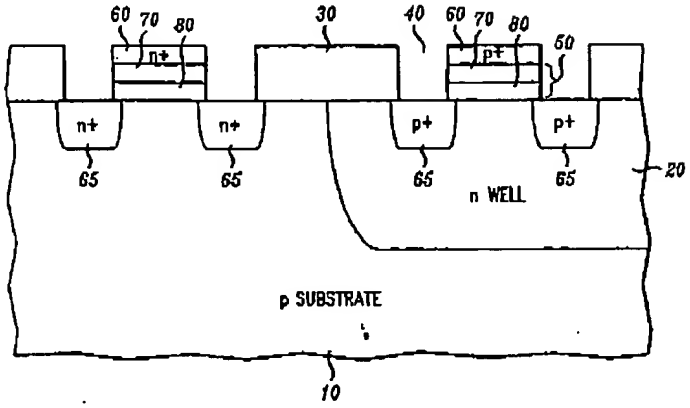
(i) forming a silicon oxynitride layer 70 on the surface of the silicon wafer 10; and

(ii) *oxidizing* the silicon substrate 10 (at a temperature of at least about 900°C.) to *grow a SiO_2 gate layer 80* under the oxynitride layer.[7]

[7] Kim at col. 4, lines 4-11 (emphasis added): "After the oxynitride layer is formed, *the silicon dioxide layer is grown. This is done by exposing the substrate to an oxidizing atmosphere at a sufficiently high temperature.* An exemplary oxidizing atmosphere contains oxygen, or, alternatively, nitrous oxide (N_2O). A temperature of at least

This process is illustrated in FIG. 1 (below) showing oxynitride layer 70 with an underlying SiO_2 gate layer 80.

FIG. 1



Thus, Kim teaches an oxynitride layer (70) that functions as a membrane for controlled ***diffusion of oxygen*** to the oxidation region of the silicon substrate (10) to form the SiO_2 gate layer (80). See the Abstract (emphasis added):

> Abstract
> A method for making gate dielectrics for MOS devices includes first forming a silicon oxynitride layer, and then forming a silicon dioxide layer that underlies the oxynitride layer. **The oxynitride layer functions as a membrane for controlled diffusion of oxygen to the oxidation region of the silicon substrate.**

In contrast, Aronowitz teaches an oxynitride layer that functions as a ***barrier to oxidation*** (at cols. 6-7, bridging paragraph; emphasis added):

> Then, the wafer is exposed to further oxidation according to methods well known in the art, such as thermal treatment. As shown in FIG. 2F, **the oxynitrides which have been formed in the region 206b of the gate dielectric act as a barrier to the oxidation process.** No such barrier exists in the un-nitridized region 206a of the gate dielectric...

about 900°C. is desirable in order to avoid compressive stress in the resulting oxide layer, and a temperature of at least about 950°C. is currently preferred."

Also see the Abstract (emphasis added):

> Abstract
> Provided is a method of fabricating gate dielectric layers having variable thicknesses and compositions over different regions of a semiconductor wafer. In a preferred embodiment of the present invention, a gate oxide layer is first grown over the various regions. Regions that are to have a relatively thicker, unhardened gate dielectric are masked and the wafer is exposed to a remote low energy nitrogen plasma. **After the nitridization process is completed, the mask is removed and the wafer is exposed to further oxidation. The regions where oxynitrides have been formed act as a barrier to the oxidation process.** Consequently, different oxide thicknesses can be grown on the same wafer, thinner and **hardened where nitridization has been performed**, and thicker and not hardened in those regions that were masked during the nitridization. Variable thickness gate dielectrics in accordance with the present invention may be particularly advantageous in semiconductor integrated circuits involving both digital and analog devices.

Clearly, one skilled in the art would have no incentive to combine the disclosure of Kim — which teaches forming an oxynitride layer that functions *to allow oxygen diffusion* to the silicon surface, with that of Aronowitz — which teaches forming an oxynitride layer that functions as a *barrier to oxygen diffusion*.

Moreover, *even if* these references were combined, they still do not teach or suggest Applicant's method as claimed.

Both Aronowitz and Kim teach forming an oxynitride layer over a silicon substrate and applying an *oxidizing* atmosphere to grow an oxide layer — *not nitridizing the oxynitride layer* to form a nitride layer, and *depositing a dielectric layer onto the nitride layer* as claimed by Applicant.

In sum, Aronowitz, either alone or combined with Kim, does not teach or suggest Applicant's method as claimed for forming a dielectric layer. Accordingly, withdrawal of the rejections of the claims is respectfully requested.

Extension of Term. The proceedings herein are for a patent application and the provisions of 37 CFR § 1.136 apply. Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that Applicant has

inadvertently overlooked the need for a petition for extension of time. If any extension and/or fee are required, please charge Account No. 23-2053.

Based on the above remarks, the Examiner is respectfully requested to reconsider and withdraw the rejections of the claims. It is submitted that the present claims are in condition for allowance, and notification to that effect is respectfully requested.

Respectfully submitted,

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Dated: September 4, 2003

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THE STAMP OF THE U.S. PATENT & TRADEMARK OFFICE HEREON DENOTES RECEIPT ON THE DATE STAMPED OF:

In re Application of:	Weimer, Ronald A.
Serial No.:	09/941,827
Confirmation No:	7551
Filing Date:	August 29, 2001
For:	Method of Improved High K Dielectric-Polysilicon Interface for CMOS Devices
Attorney Docket No.:	MTI-31532

Enclosures: Response to Restriction Requirement and Preliminary Amendment, Replacement Claims, Blackline Claims, Supplemental Information Disclosure Statement, Form 1449, copy of references, Transmittal, Check No. 157718 for $870.00 (claims fees), and return postcard.

Date: December 3, 2002 Express Mail No. EV 048318230 US

PRR/KXS

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